from an expansion base for remote computing operations. The expansion base when used typically provides expandability for functions not included in the laptop portion L due to space or power concerns. The laptop computer L may be of a type which is not connectable to an expansion base, as well. While the laptop computer L is docked into an expansion base or otherwise connected by at a power supply inlet **90** (FIGS. **2** and **6**) to alternating current power, the laptop computer L operates on AC power. Rechargeable batteries in a rechargeable power supply **92** are also being recharged at this time. When computer L is detached from the source of AC power, the rechargeable power supply **92** (FIG. **2**) provides power and the laptop computer L operates from battery power.

The Central Processing Unit (CPU) **100** is provided in the laptop computer L which is a conventional microprocessor such as the Pentium® from Intel Corporation or a similar processor. The CPU **100** couples to a host bus **110** for communicating with system logic such as a cache memory **102**, a Mobile Peripheral Component interconnect bus cache controller (MPC) **108** and pair of Mobile Data Buffers (MDB) **104**. The cache memory **102** is a conventional cache memory for the CPU **100** and preferably employs high speed synchronous burst static Random Access Memory (RAM). The MPC **108** provides an interface to the cache memory **102**, and includes tag RAMs and other logic for creating various cache ways, size, and speed configurations of the cache memory **102**.

The MPC **108** and the MDB **104** are also coupled to a system memory **106** and a peripheral component interconnect (PCI) bus **112**. The MPC **108** provides address and control to system memory **106**, which is typically comprised of up to 256 MByte of conventional dynamic random access memories (DRAMs). The MDB **104** provides a 64 bit data path between the host bus **110** and the system memory **106** and provides a 32-bit data path to the PCI bus **112**. The MPC **108** and MDB **104** have three major functional interfaces: a processor/cache interface, a system memory interface, and a PCI bus interface. The MDB **104** is responsible for buffering data between the three interfaces while the MPC **108** is responsible for handling addressing, command and control. Each of these interfaces operate independently from the other and includes queues for read and write posting between any two of the three interfaces. The processor/cache interface allows the CPU **100** to pipeline cycles into read cycles and allows snoop accesses to the tag RAM to occur while the pipeline cycles are executing. The memory interface controls the system memory **106** and generates control signals to the MDB **104**. The interface also allows read ahead operations for those PCI masters issuing a read multiple command. The PCI interface allows MPC **108** to act as a PCI master when the CPU **100** is accessing the PCI bus **112**, or as a PCI slave when a PCI device accesses system memory **106**.

The PCI bus is designed to have a high throughput and to take advantage of an increasing number of local processors supporting I/O functions. For example, most disk controllers, particularly Small Computer System Interface (SCSI) controllers, and network interface cards (NICs) include a local processor to relieve demands on the host processor. Similarly, video graphics boards often include intelligent graphics accelerators to allow higher level function transfer. Typically these devices incorporate the capability to act as bus masters, allowing them to transfer data at the highest possible rates. As mentioned, potential bus masters include the CPU/main memory subsystem (via MPC **108**).

The PCI bus **112** provides a communications conduit between the laptop computer L and an expansion base. The PCI bus **112** in the laptop computer L includes a Quickswitch **113** for each signal of the PCI bus **112**. In the preferred embodiment, the Quickswitches **113** are low loss series in-line MOSFET devices with the gate (control line) driven by a control signal CONTROL from a Mobile Super Input Output Logic or MSIO-L **124**. The Quickswitch **113** can thereby be used to facilitate hot plug capabilities. When the laptop computer L is docked into an expansion base and the Quickswitches **113** are turned on, an extension portion of the PCI bus **112** present in the expansion base is coupled to the PCI bus **112** via expansion connector **146** to provide the extended PCI bus **112**. Details of the expansion connector **146** and associated docking/undocking logic are provided in commonly owned co-pending U.S. patent application Ser. No. 08/684,255 entitled "COMPUTER SYSTEM INCORPORATING HOT DOCKING AND UNDOCKING CAPABILITIES WITHOUT REQUIRING A STANDBY OR SUSPEND MODE" filed Jul. 19, 1996, which is incorporated herein by reference.

In the laptop computer L, the PCI bus **112** further couples to a video graphics controller **114**, a Cardbus interface **116** and a Mobile Integrated System Controller—Laptop **118** (MISC-L). The video graphics controller **114** further couples to a low power liquid crystal display (LCD) **121** or alternatively a cathode ray tube (CRT) or any other suitable monitor. The video graphics controller **114** is also provided with an output terminal **115** (FIGS. **2** and **6**) for driving an external video monitor. The Cardbus interface **116** is provided for communicating with add-on cards **120** such as networking cards, modem cards, solid state storage cards and rotating storage cards preferably of a Personal Computer Memory Card International Association (PCMCIA) style. The MISC **118** provides an interface for an Industry Standard Architecture (ISA) bus **138**, and an integrated drive electronics (IDE) hard drive interface for communicating with hard drives **122**. The MISC **118** is also configurable based on an input pin for use in the laptop computer L and is further coupled to the internal ISA bus **138**.

The MISC **118** bridges the PCI bus **112** to the ISA bus **138** or an ISA bus in the expansion base. The MISC **118** acts as both a master and slave on the PCI bus **112** and a bus controller on the ISA buses. The MISC I**18** further preferably includes bus arbitration circuitry whose details are contained in commonly owned, co-pending application Ser. No. 08/684,255 incorporated by reference above.

In the preferred embodiment of the invention, the MISC **118** also as is conventional incorporates **8237** compatible direct memory access (DMA) controllers, an enhanced DMA controller for fast IDE hard drives, **8254** compatible timers, an **8259** compatible interrupt controller, hot docking support logic, system power management logic, and Plug-and-Play support.

The MISC **118** and the ISA bus **138** provide support for standard ISA peripherals such as those combined in a Mobile Super Input/Output (MSIO) **124** peripheral. The MSIO **124** peripheral has a combination of standard ISA peripherals, such as: a 146818 compatible real time clock (RTC), a floppy controller for interfacing to standard floppy drives **130**; an **8051** compatible microcontroller for communicating with a standard keyboard **132**, a conventional infrared communication input receiver **133** (FIGS. **2** and **6**) and pointing device **150** (FIG. **2**), for performing scanning and key code conversions on the keyboard **132**, and for performing power management and hot docking functions; a universal asynchronous receiver transmitter (UART) for